WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a chip on which an integrated circuit is formed;

a differential output driver circuit which externally outputs a pair of differential signals generated by the integrated circuit;

first and second signal lines which transmit the pair of differential signals output from the differential output driver circuit; and

a delay unit which is connected in the chip to at least one of the first and second signal lines, has an active element for delaying signals passing through the first and second signal lines so as to make delays of the signals substantially equal to each other, and compensates for a signal delay time generated by a line length difference between the first and second signal lines.

2. The device according to claim 1, wherein the delay unit includes a capacitance element having one electrode connected to a signal line with a shorter line length out of the first and second signal lines, and the capacitance element includes a capacitance element using a MOS (Metal-Oxide-Semiconductor) gate capacitance.

3. The device according to claim 1, wherein the delay unit can change a delay time.

4. The device according to claim 3, wherein the delay unit comprises a plurality of capacitance elements, and a control circuit which is interposed between a signal line with a shorter line length out of the first and second signal lines and one electrode of each of said plurality of capacitance elements and selectively applies a potential to said one electrode of each of said plurality of capacitance elements.

5. The device according to claim 3, wherein the delay unit comprises a plurality of capacitance elements, a plurality of switching elements each of which is connected between one electrode of a corresponding one of said plurality of capacitance elements and a signal line with a shorter line length out of the first and second signal lines, and a control circuit which selectively ON/OFF-controls said plurality of switching elements.

6. The device according to claim 3, wherein the delay unit comprises a plurality of capacitance elements each having one electrode connected to a signal line with a shorter line length out of the first and second signal lines, and a control circuit which selectively applies a potential to the other electrode of each of said plurality of capacitance elements.

7. The device according to claim 1, further comprising an input/output circuit which is arranged in the chip and has at least one of an input and output

not terminated with impedance matching.

8. The device according to claim 1, in which the delay unit comprises a control circuit that controls a delay time, and

which further comprises a receiving circuit that is arranged in the chip and receives correction data having passed through the first and second signal lines, a signal selecting circuit which receives an output signal from the receiving circuit and a control signal and supplies a selected signal to the control circuit, and a switching signal generator which supplies a switching signal to the signal selecting circuit.

9. The device according to claim 1, in which the delay unit comprises a control circuit that controls a delay time, and

which further comprises a test unit that controls the control circuit and checks a margin for unbalance between the pair of differential signals.

10. The device according to claim 9, wherein the test unit includes a test signal generation circuit which is arranged in the chip, generates a test signal, and supplies the test signal to the control circuit.

11. The device according to claim 9, wherein the test unit includes a tester which is connected to the first and second signal lines, determines a difference between the pair of differential signals, and checks

a margin for a delay amount.

12. A semiconductor integrated circuit device comprising:

a chip on which an integrated circuit is formed;

a differential output driver circuit which externally outputs a pair of differential signals generated by the integrated circuit;

first and second signal lines which transmit the pair of differential signals output from the differential output driver circuit; and

a delay unit which is connected in the chip to at least one of third and fourth signal lines which transmit the pair of differential signals from the integrated circuit to the differential output driver circuit, has an active element for delaying at least one of the pair of differential signals so as to make delays of the signals passing through the first and second signal lines substantially equal to each other, and compensates for a signal delay time generated by a line length difference between the first and second signal lines.

13. The device according to claim 12, wherein the delay unit includes a capacitance element having one electrode connected to a signal line with a shorter line length out of the first and second signal lines on the third and fourth signal lines, and the capacitance element includes a capacitance element using a MOS

(Metal-Oxide-Semiconductor) gate capacitance.

14. The device according to claim 12, wherein the delay unit can change a delay time.

15. The device according to claim 14, wherein the delay unit comprises a plurality of capacitance elements, and a control circuit which is interposed between a signal line with a shorter line length out of the first and second signal lines on the third and fourth signal lines and one electrode of each of said plurality of capacitance elements and selectively applies a potential to said one electrode of each of said plurality of capacitance elements.

16. The device according to claim 14, wherein the delay unit comprises a plurality of capacitance elements, a plurality of switching elements each of which is connected between one electrode of a corresponding one of said plurality of capacitance elements and a signal line with a shorter line length out of the first and second signal lines on the third and fourth signal lines, and a control circuit which selectively ON/OFF-controls said plurality of switching elements.

17. The device according to claim 14, wherein the delay unit comprises a plurality of capacitance elements each having one electrode connected to a signal line with a shorter line length out of the first and second signal lines on the third and fourth signal lines, and a control circuit which selectively applies

a potential to the other electrode of each of said plurality of capacitance elements.

18. The device according to claim 14, wherein the delay unit comprises first and second flip-flop circuits which receive the pair of differential signals having passed through the third and fourth signal lines from the integrated circuit, and a control circuit which supplies clock signals to the first and second flip-flop circuits.

19. The device according to claim 12, further comprising an input/output circuit which is arranged in the chip and has at least one of an input and output not terminated with impedance matching.

20. The device according to claim 12, in which the delay unit comprises a control circuit that controls a delay time, and

which further comprises a receiving circuit that is arranged in the chip and receives correction data having passed through the first and second signal lines, a signal selecting circuit which receives an output signal from the receiving circuit and a control signal and supplies a selected signal to the control circuit, and a switching signal generator which supplies a switching signal to the signal selecting circuit.

21. The device according to claim 12, in which the delay unit comprises a control circuit that controls

a delay time, and

which further comprises a test unit that controls the control circuit and checks a margin for unbalance between the pair of differential signals.

22. The device according to claim 21, wherein the test unit includes a test signal generation circuit which is arranged in the chip, generates a test signal, and supplies the test signal to the control circuit.

23. The device according to claim 21, wherein the test unit includes a tester which is connected to the first and second signal lines, determines a difference between the pair of differential signals, and checks a margin for a delay amount.

24. A system using a semiconductor integrated circuit device, comprising:

a semiconductor integrated circuit device comprising a differential output driver circuit which externally outputs via first and second signal lines a pair of differential signals generated within a chip;

a first receiving unit which receives the pair of differential signals output from the semiconductor integrated circuit device via the first and second signal lines;

a signal processing unit which processes the pair of differential signals received by the first receiving unit and generates correction data for correcting unbalance between the pair of differential signals;

a transmitting unit which transmits the correction data generated by the signal processing unit to the semiconductor integrated circuit device;

a second receiving unit which is arranged in the semiconductor integrated circuit device and receives the correction data transmitted from the transmitting unit; and

a delay unit which changes a delay time on the basis of the correction data received by the second receiving unit, has an active element for delaying signals passing through the first and second signal lines so as to make delays of the signals substantially equal to each other, and compensates for a signal delay time generated by a line length difference between the first and second signal lines.

25. The system according to claim 24, further comprising a test unit which controls the delay unit and checks a margin for unbalance between the pair of differential signals.

26. The system according to claim 25, wherein the test unit includes a test signal generation circuit which is arranged in the chip, generates a test signal, and supplies the test signal to the delay unit.

27. The system according to claim 26, wherein the test unit includes a tester which is connected to the first and second signal lines, determines a difference between the pair of differential signals, and checks

a margin for a delay amount.

28. The system according to claim 24, wherein the delay unit is inserted in at least one of the first and second signal lines.

29. The system according to claim 28, wherein the delay unit is inserted in at least one of third and fourth signal lines in an internal circuit which supplies the pair of differential signals to the differential output driver circuit.

30. The system according to claim 24, wherein the delay unit comprises first and second flip-flop circuits, and a control circuit which supplies clock signals in different phases to the first and second flip-flop circuits, and the control circuit is controlled on the basis of the correction data received by the second receiving unit.

31. The system according to claim 30, wherein the second receiving unit comprises a receiving circuit which receives the correction data output from the transmitting unit, a signal selecting circuit which receives the correction data received by the receiving circuit and a control signal, selects one of the correction data and the control signal, and supplies a selected signal to the control circuit, and a switching signal generator which supplies a switching signal to the signal selecting circuit and controls selection.

32. The system according to claim 31, wherein

the receiving circuit receives the correction data which is output from the transmitting unit and transmitted through the first and second signal lines.

33. The system according to claim 24, wherein the delay unit comprises a plurality of capacitance elements, and a control circuit which selects said plurality of capacitance elements and controls the delay time, and the control circuit is controlled on the basis of the correction data received by the second receiving unit.

34. The system according to claim 33, wherein the second receiving unit comprises a receiving circuit which receives the correction data output from the transmitting unit, a signal selecting circuit which receives the correction data received by the receiving circuit and a control signal, selects one of the correction data and the control signal, and supplies a selected signal to the control circuit, and a switching signal generator which supplies a switching signal to the signal selecting circuit and controls selection.

35. The system according to claim 34, wherein the receiving circuit receives the correction data which is output from the transmitting unit and transmitted through the first and second signal lines.